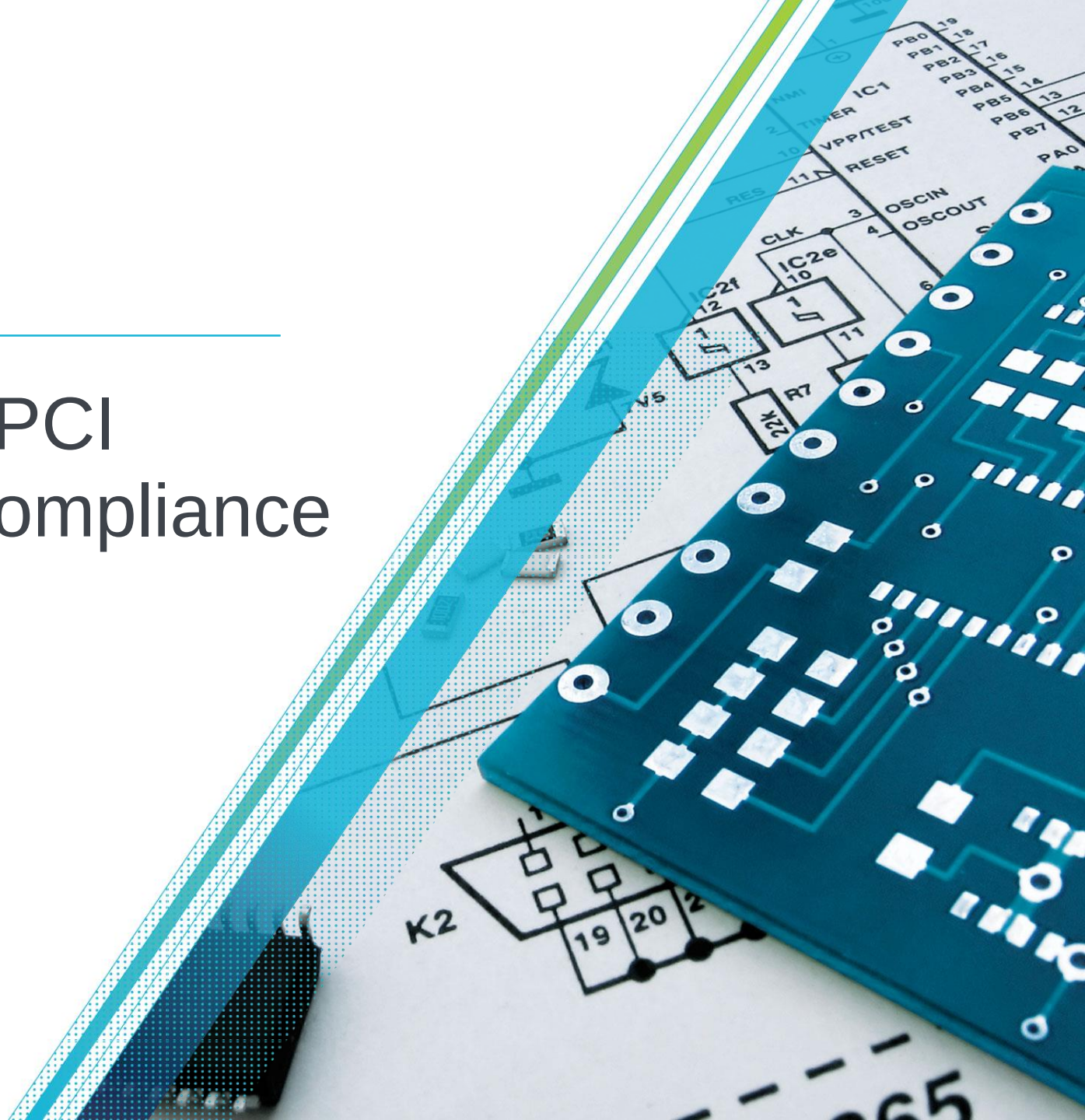
Tektronix

Achieving PCI Express Compliance Faster



Agenda

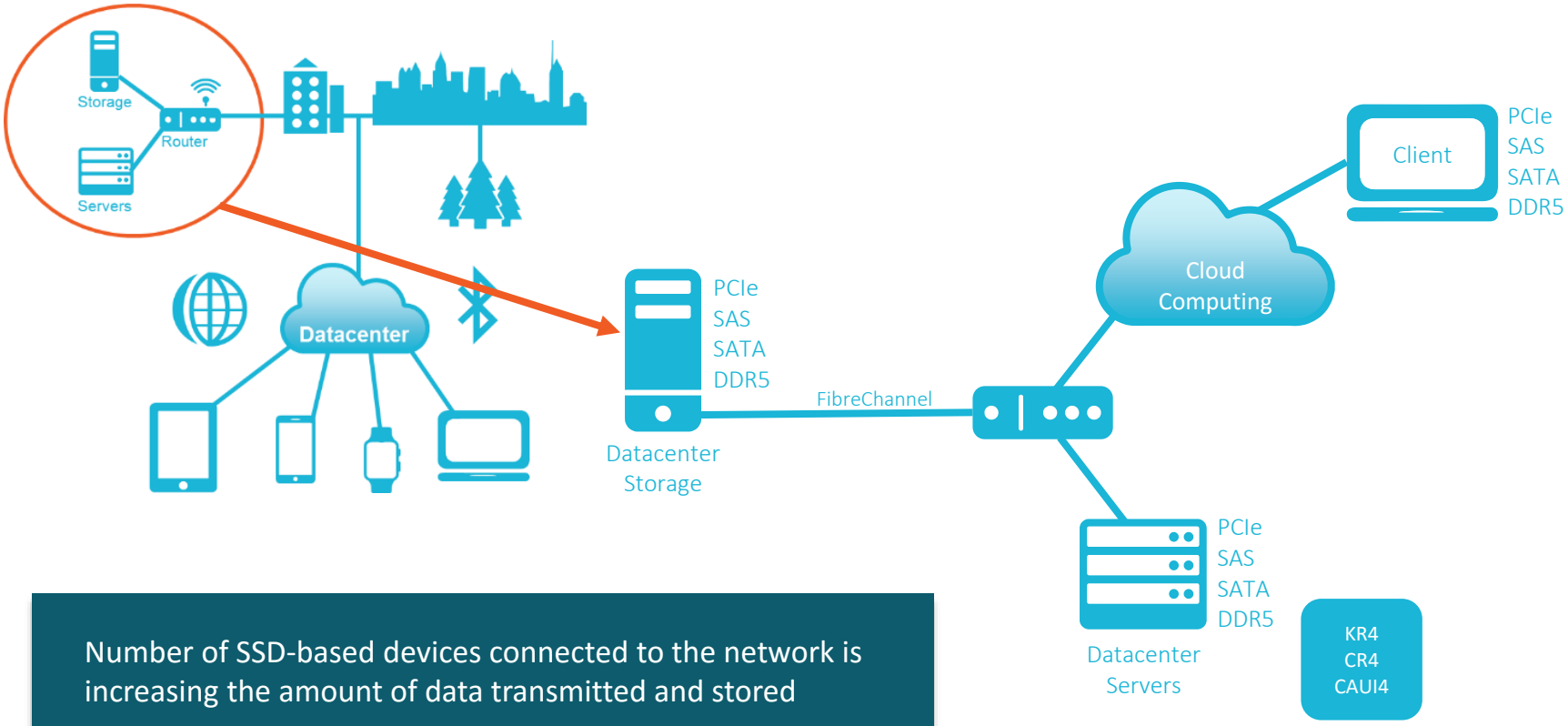
- PCIe Overview including what's new with Gen4
- PCIe Transmitter Testing
- PCIe Receiver Testing
- Intro to Tektronix's PCIe Tx and Rx Test Solution

PCIe Market Intro

- PCI Express is a **high performance, general purpose I/O interconnect** used in a wide variety of computing & communications products. It has become especially popular for NVME SSD applications
- PCIe is based upon a **point-to-point bus topology** between a root-complex (system/host) & an end-point (add-in card) that supports full-duplex communications.
- The PCIe physical layer consists of:
  - Differential low-voltage signaling
  - **100MHz RefClk is either Common or Separate** (SRIS/SRNS)
  - **Scalable widths:** x1, x2, x4, x8, x12, x16, x32
  - **Scalable speeds**: 2.5GT/s (Gen1), 5GTs (Gen2), 8GT/s (Gen3), 16GT/s (Gen4)
  - **Utilizes connectors**, e.g., CEM, U.2 (SFF-8639), M.2 or soldered directly to PCB
- Specifications are developed & maintained by the **PCI-SIG,** a consortium of >900 companies.

Technology Overview

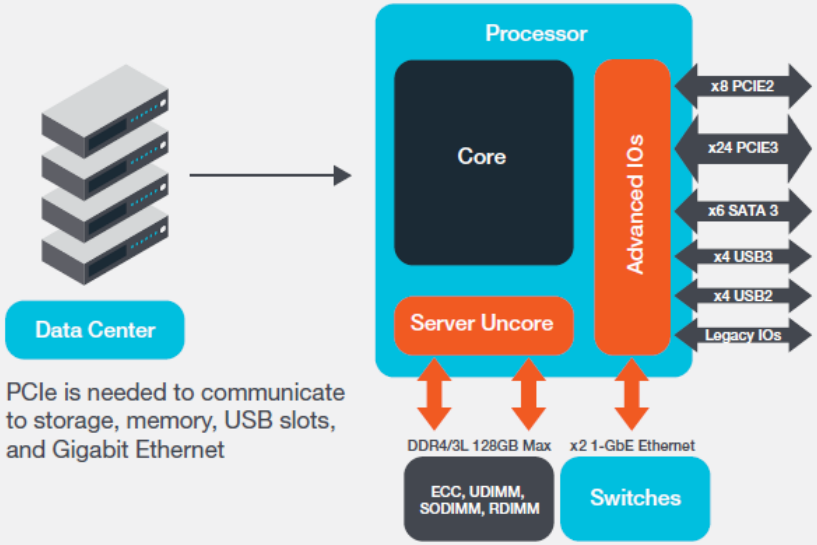
BIG DATA, IOT AND ANALYTICS DRIVING NEED FOR COMPUTE POWER, STORAGE CAPACITY, AND NETWORK BANDWIDTH



Number of SSD-based devices connected to the network is increasing the amount of data transmitted and stored

PCI Express Overview

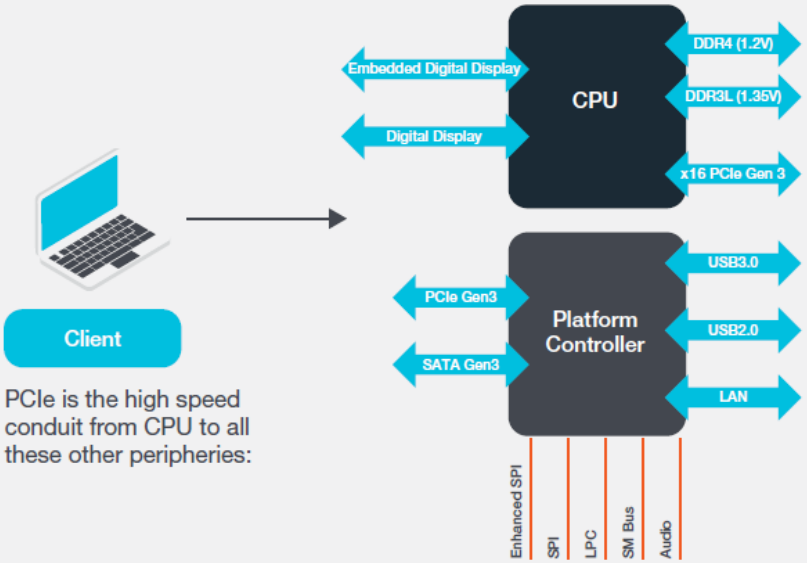
Architecture and Neighboring Technologies



PCIe is needed to communicate to storage, memory, USB slots, and Gigabit Ethernet

For Data Centers PCIe interfaces with these other standards:

- SATA
- DDR
- USB
- 10GbE



PCIe is the high speed conduit from CPU to all these other peripheries:

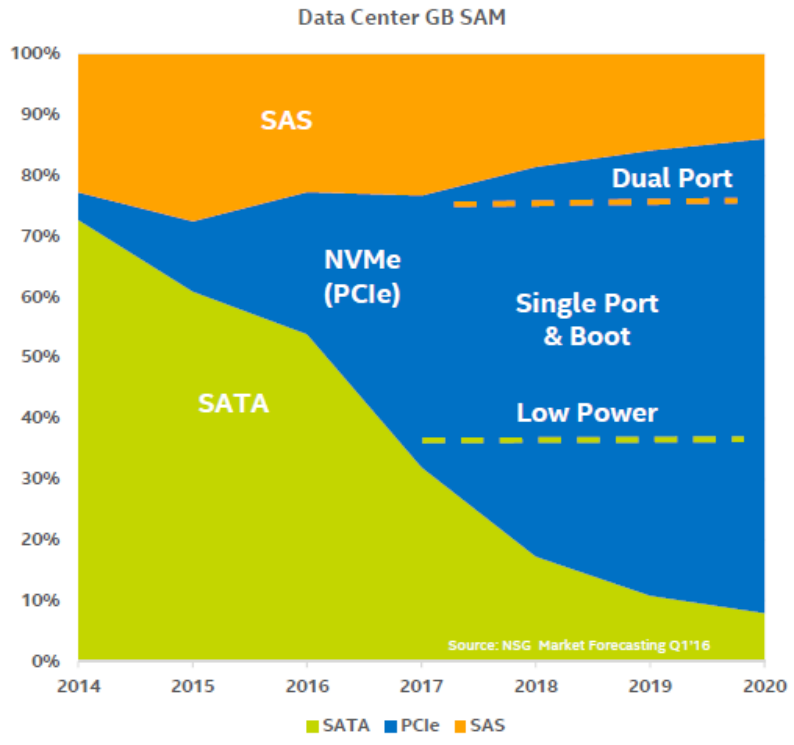
For the Client PCI Express interfaces with these other standards:

- SATA
- DDR
- USB
- Thunderbolt
- DisplayPort
- HDMI

PCI Express is emerging as the primary, high-performance storage bus and SSD Interface

PCIe SSD Forecasted to Lead in Datacenter

EXPECTED TO OVERTAKE SAS IN 2017 & SATA IN 2018



Source: Q1'16 Intel NSG Market Forecasting

- PCI Express (PCIe) projected as leading SSD interface in DC by 2017
- PCIe bandwidth is significantly higher than SAS or SATA
- NVM Express (NVMe--SW interface) has lower latency than SAS or SATA
- Increasing focus on *scalability* using protocol-driven dynamic cloud management and virtual storage--decreasing CPU overhead and improving performance

PCIe Compliance Testing

PCIe COMPLIANCE TESTING FOR INTEROPERABILITY

- PCIE holds regular compliance workshops/plugfests to certify individual devices' compliance and interoperability, typically 4x/yr
- Vendors who desire to be on PCI-SIG Integrator's List plan to attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests
- These vendors look at tests and test equipment and assume that if they buy & use the same equipment, they will pass the workshop electrical tests

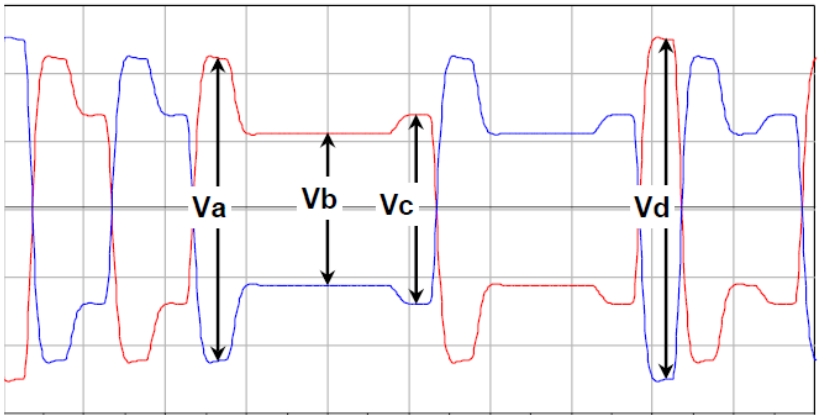
PCIE 3.0 Electrical PHY Compliance Tests
Transmitter Testing
Receiver Jitter Tolerance Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing

For more details visit PCI Compliance program:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical30

Compliance Equalization Presets

- Once in compliance mode, bursts of 100 MHz clock can be used to cycle through various settings of compliance patterns to perform **automated** jitter, voltage, timing measurements.
- 11 presets for both Gen3 and Gen4 (22 total). All preset values must be supported by DUT.
- For Rx AIC testing, BER < 1E-12 while receiving any valid preset/TXEQ, or < 1E-4 while receiving either P7 or P8

Preset #	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	Variable[1]



De-emphasis = 20 $\log_{10}$Vb/Va
Preshoot = 20$\log_{10}$Vc/Vb
Boost = 20$\log_{10}$ Vd/Vb

1. P10 levels are not fixed; its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used to test the boost level of the Tx during full swing

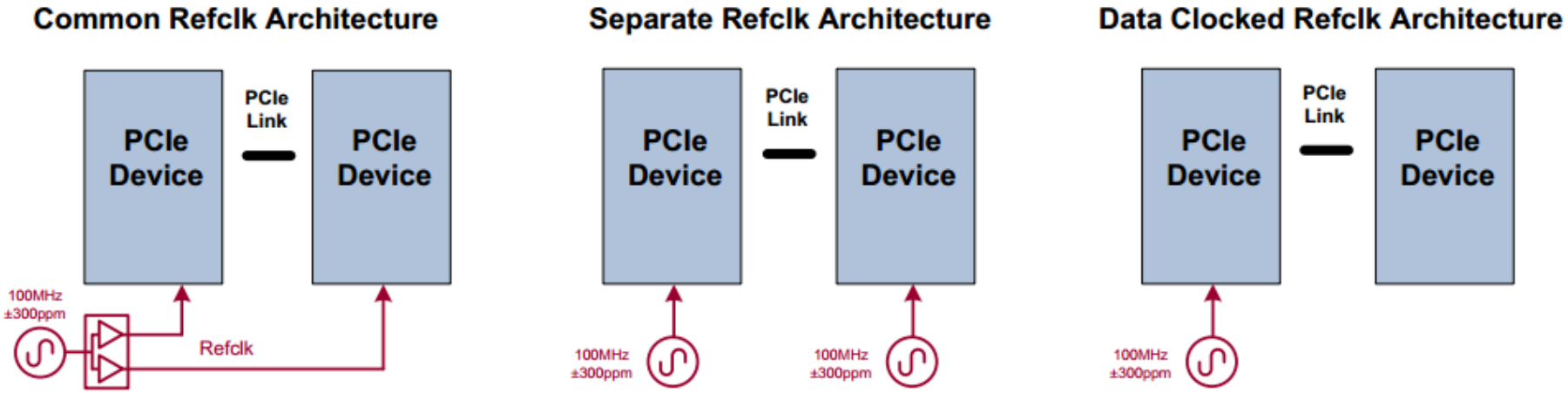
PCIe Gen4 Overview

KEY ENHANCEMENTS FROM PCIe GEN3

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Reduction in RJ (random jitter) from 3ps (PCIe3) to ~1ps (PCIe4) *[PCIe Base Spec, Table 9.8]*
  - Maintains backward compatibility w/ PCIe installed base of devices
  - Gen4 connector enhanced electrically
  - Behavioral Rx EQ data rate dependent
  - Limited channel: ~12" for 1 connector (including 4" AIC); requires use of repeater (both redriver & retimer) for longer channels and/or 2nd connector
  - New 'SRIS' independent RefClk modes
    - SRNS – Separate RefClk Independent with No SSC Architecture
    - SRIS – Separate RefClk Independent with SSC Architecture
  - New Rx Lane Margining feature measures EH/EW margin at end of channel
  - Eye height for Gen4 reduced to 15mVpp
- Rev 0.9 Base spec draft to be finalized in Q1 2017
- Gen4 CEM Spec currently at released at rev 0.5, draft 0.7 in process

PCIe RefClk Architectures

- PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices and support for three distinct clocking architectures:



- **Common** – most popular, supports SSC; same clock must be connected to all devices while maintaining skew <= 12 ns between devices
- **Separate/independent** – used for cabled applications; SSC not recommended unless both clocks synchronized to a common source
- **Data Clocked** – simplest to implement, but not very common

"Selecting the Optimum PCI Express Clock Source", Figure 3 page 3, Silicon Laboratories, Inc.

PCI Express Form Factors

CEM Add-In-Card (AIC)

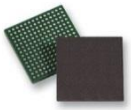
U.2 (SFF-8639)

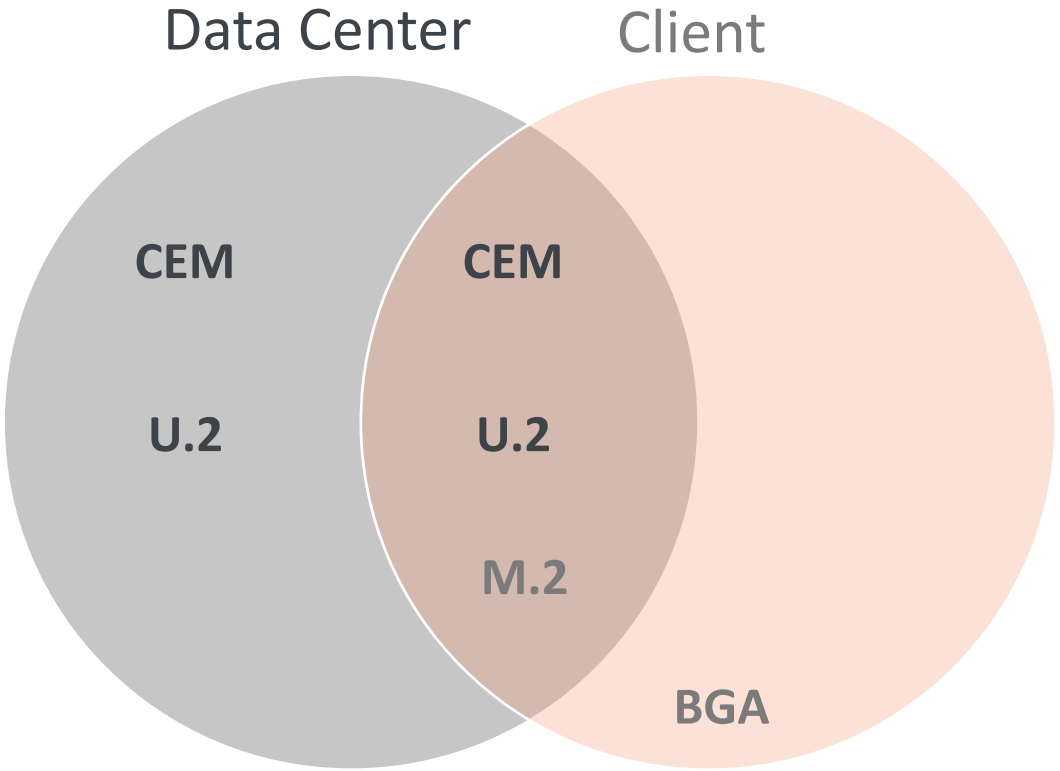
U.2-to-CEM Adapter

M.2

M.2-to-CEM Adapter

BGA *(Embedded)*

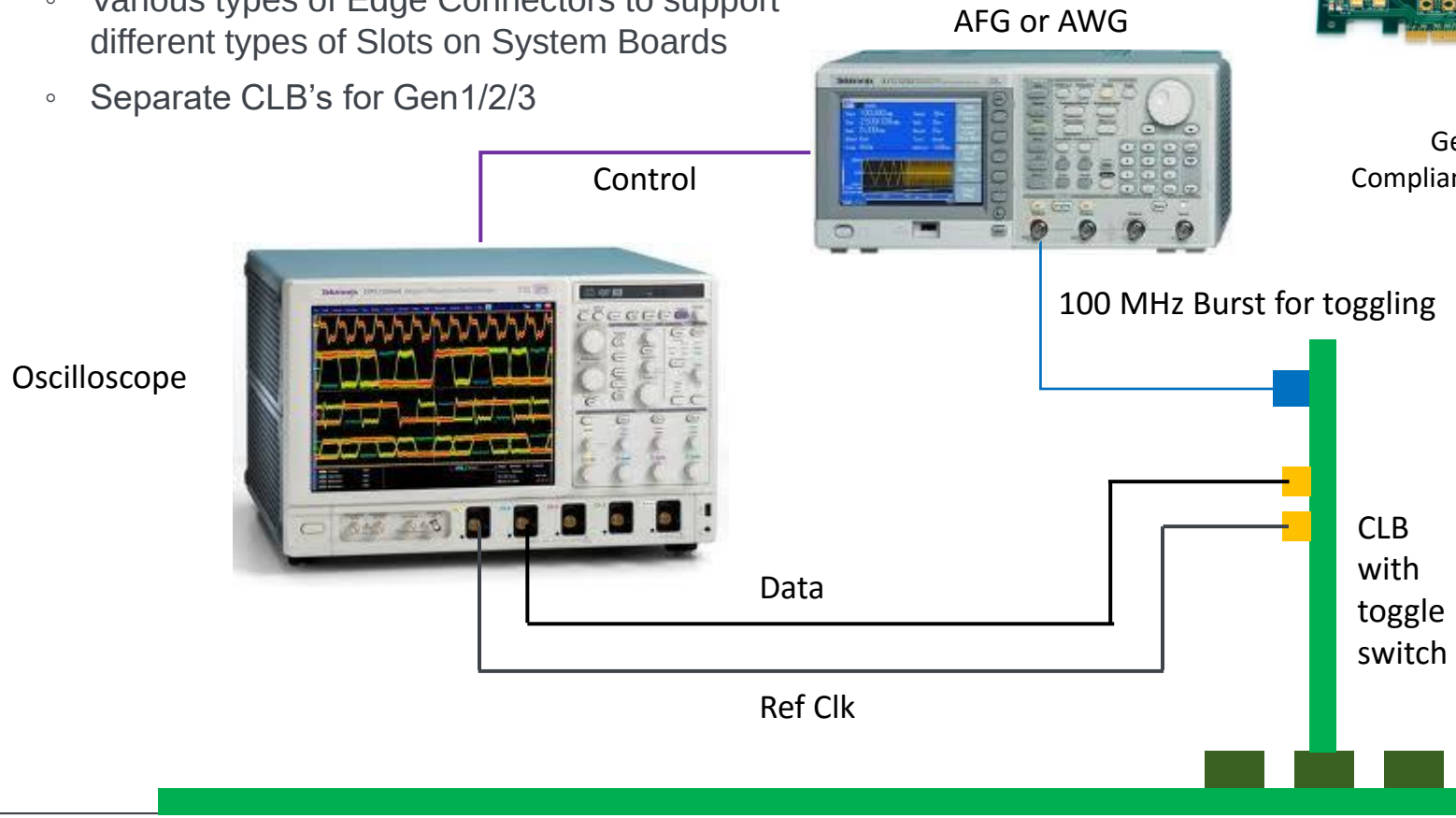




Automated DUT Control with Fixtures

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3

Gen3 CEM
Compliance Load Board
(CLB3)

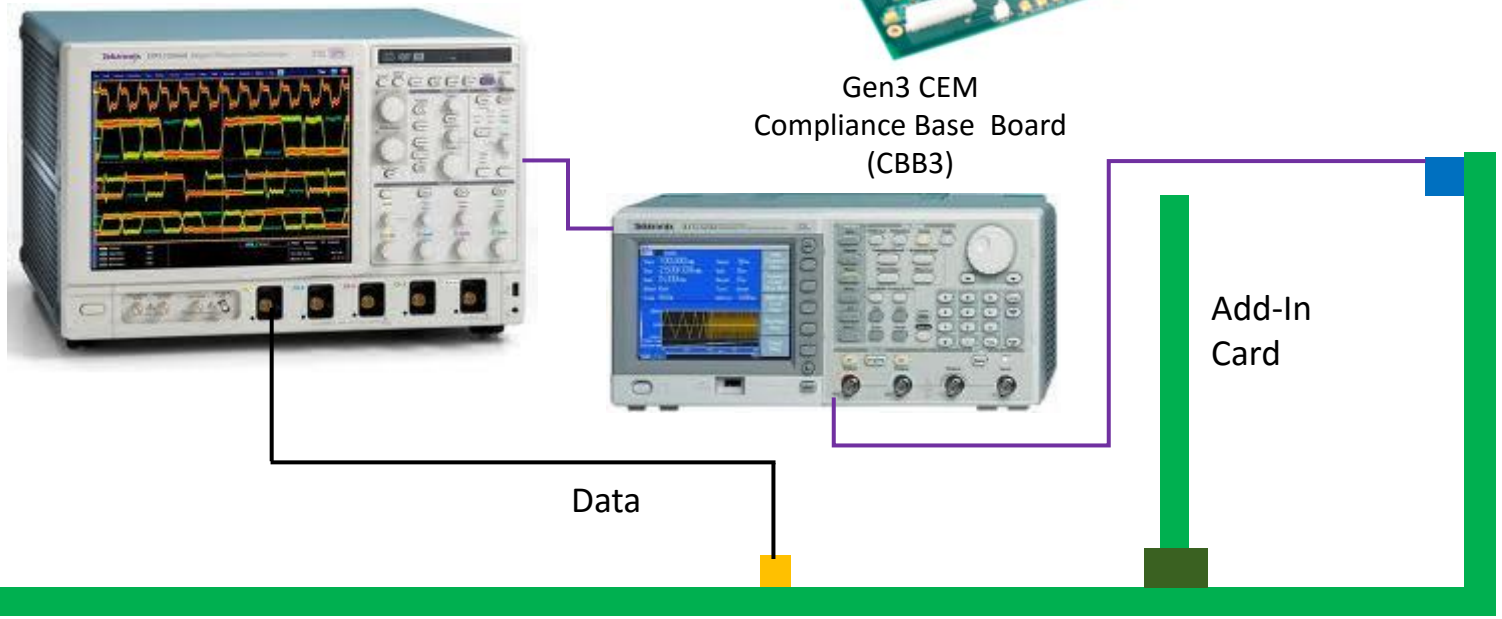


Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Gen3 CEM
Compliance Base Board
(CBB3)

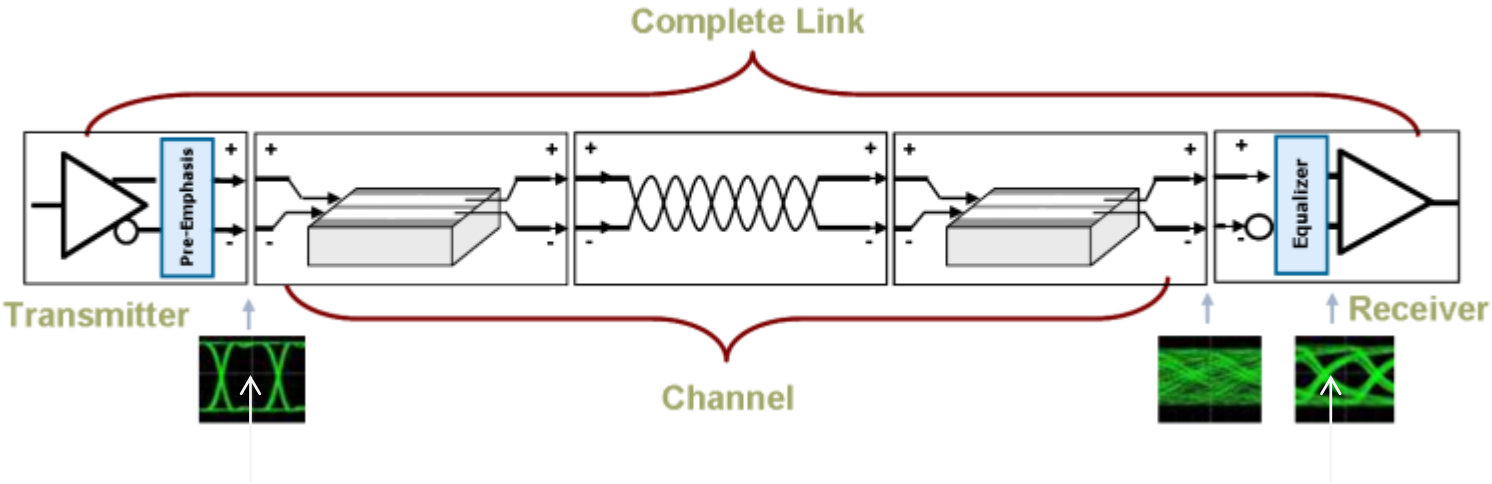
Gen3 U.2
Compliance Base Board
(CBB3)



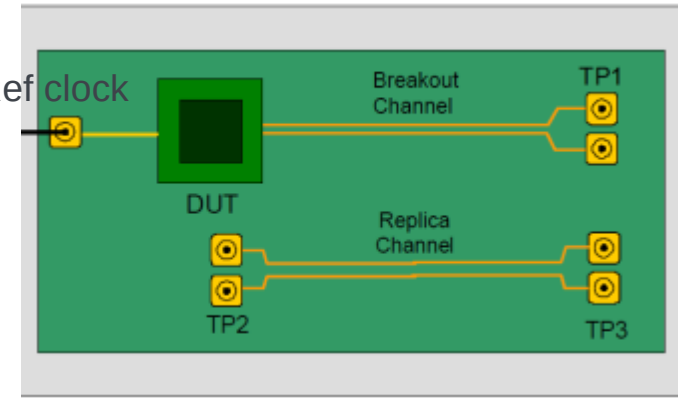
CBB with Multiple Slots of different widths and toggle switch

Form Factor Overview

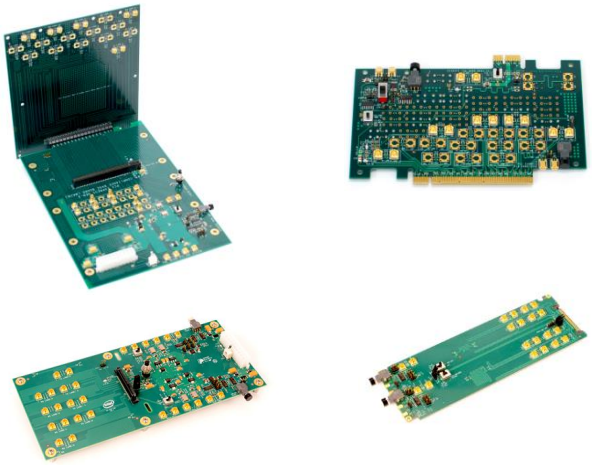
PCIe BASE vs FORM FACTOR (CEM / U.2)



Measure for Base



Measure for CEM & U.2

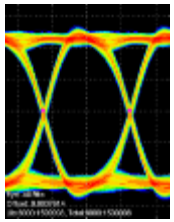


Measuring the signal at the point of interest

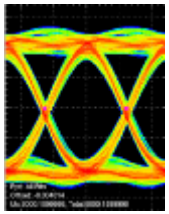
Base Spec Tx Testing

SILICON LEVEL

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel
- Measurement at TX pins can also be enabled by high fidelity probes, eg P7700

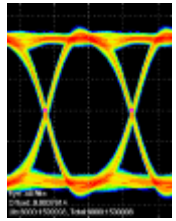


Signal at Tx Pins

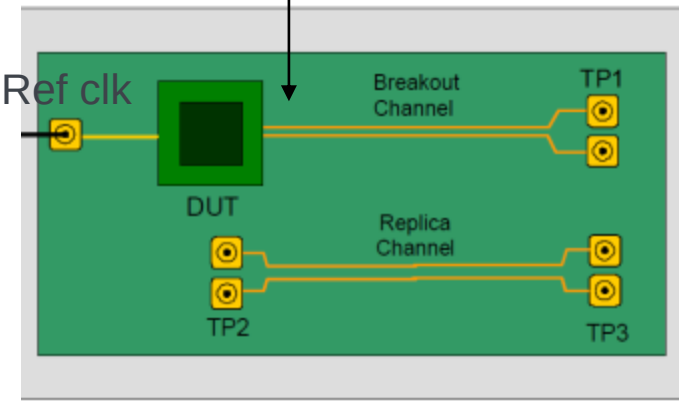


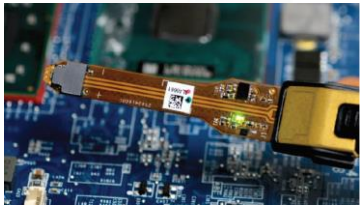
Measured Signal at TP1

De-embed using S-Parameters



Signal with Channel Effects Removed

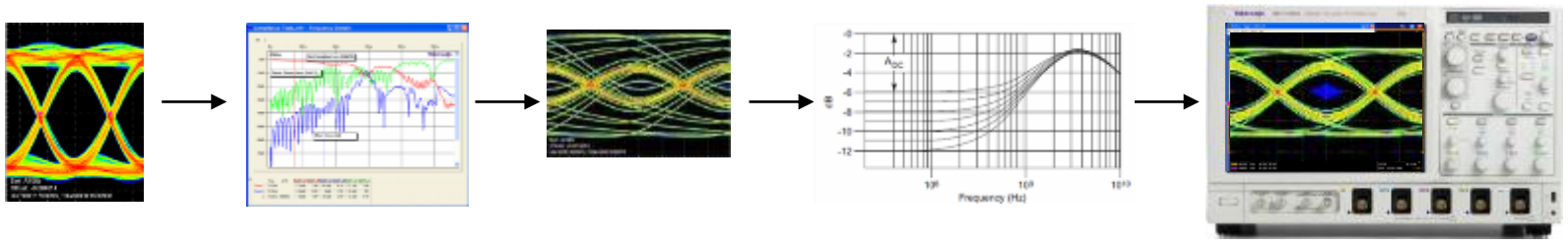




CEM & U.2 Spec Tx Testing

SYSTEM & ADD-IN CARD

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



Signal Acquired from Compliance Board

Embed Compliance Channel and Package

Closed Eye due to the Channel

Apply CTLE + DFE

Open Eye for Measurements

New Challenges in Rx Testing

PHY AND PROTOCOL-AWARE TEST AND DEBUG

Requires Protocol Awareness

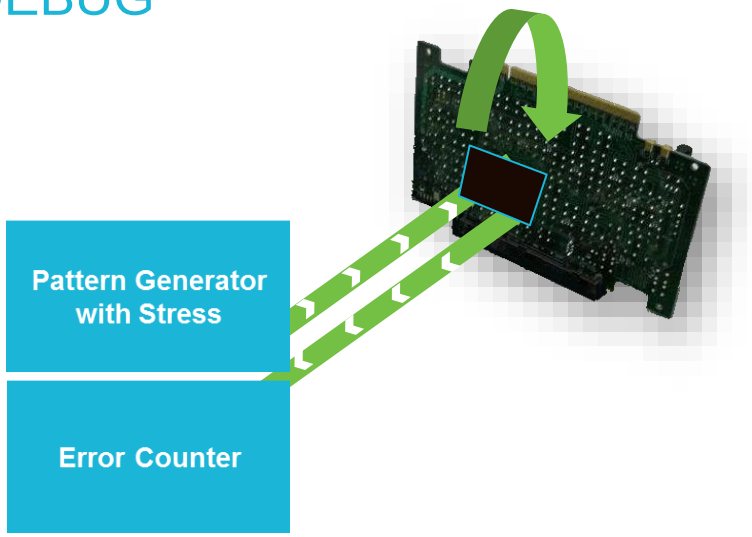
1. Putting device into loopback
2. Performing link equalization

Need Automated Solutions for Gen3 and Gen4 Standards

3. Easy setup
4. Auto calibration of stresses.
5. Making accurate and repeatable measurements

Go beyond compliance

6. Root-causing factors leading to bit-error or link training problems



ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	

New Challenges in Rx Testing

PHY AND PROTOCOL-AWARE TEST AND DEBUG

- Repeater IC's increasingly important to improve signal integrity
  - Increasingly lossy channels and increasing data rates (**-28dB** for PCIe Gen4 CEM)
  - **Need to open eye at end of the channel!**
  - Different types of repeater IC's used:
    - *Redriver—no clock-data recovery (CDR)*
    - *Clock-synchronous retimer—has CDR, clocks data to recovered clock*
    - *Clock-compensating retimer—has CDR, clocks data to ref clock*
  - Repeaters include some combination of SERDES, CDR, and CTLE/DFE equalization capability to open eye after lossy channel
    - *CTLE = continuous time linear equalization*
    - *DFE = decision feedback equalizer*

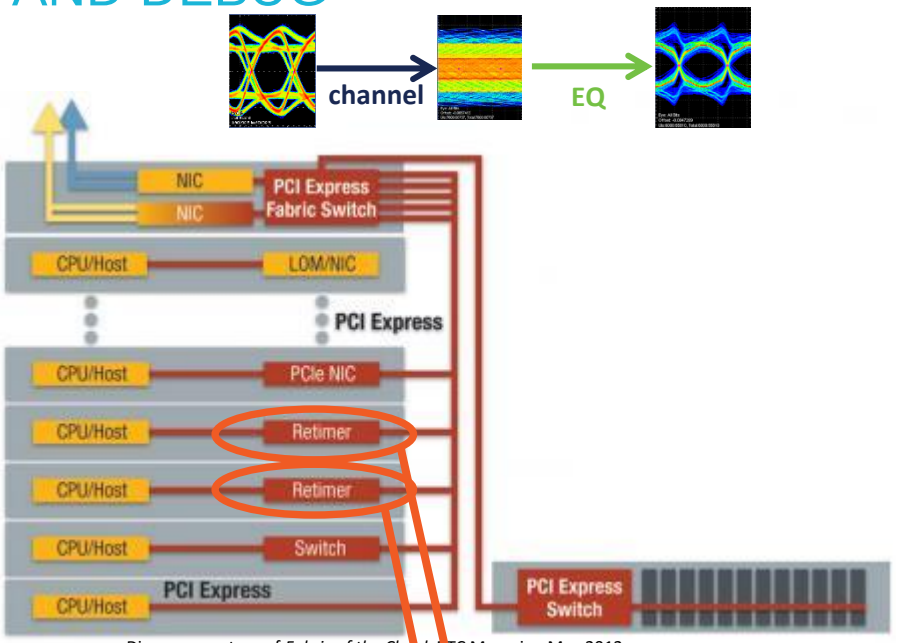


Diagram courtesy of *Fabric of the Cloud,* HTC Magazine May 2012

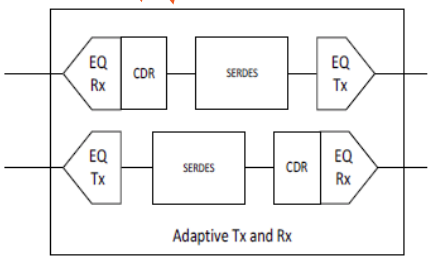
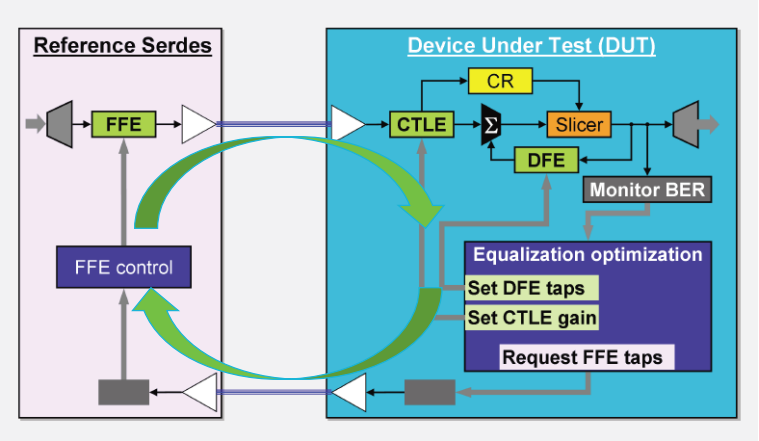


Diagram courtesy of *Proposed Concepts for SPL-5 to improve design flexibility and connectivity,* Microsemi, Nov 2016

New Challenges in Rx Testing

PHY AND PROTOCOL-AWARE TEST AND DEBUG

- Entire link (including repeaters) requires link training capability.
  - Adaptive, optimizing equalization that requires coordination of Tx and Rx for each link at power up and recovery
  - Precise orchestration of FFE, CTLE, CR, slicer, and DFE functionality is essential,
  - Data stream/protocol management (scrambling, sequencing, encoding test patterns)
- NRZ (non-return to zero) symbol decoders/bit slicers with 15mVpp sensitivity.
- Some standards (eg SAS4) also use forward error correction (FEC) to relax bit error rate (BER) requirements, but also complicate measurements.

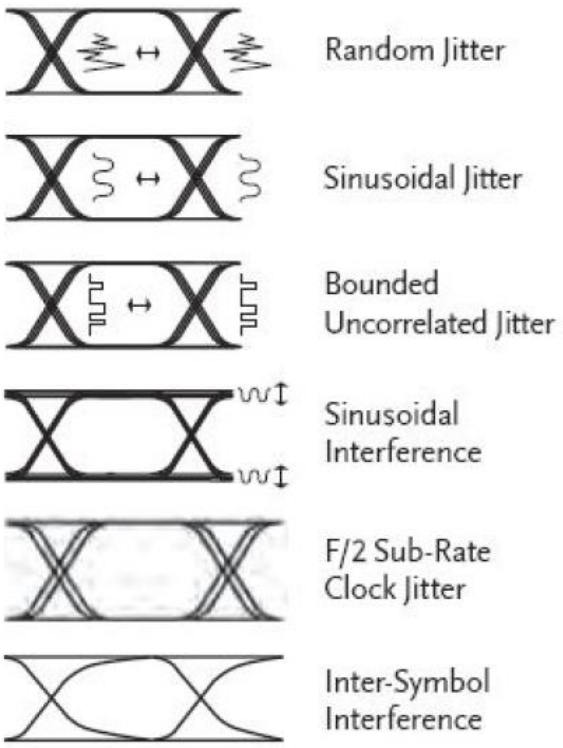


New Challenges in Rx Testing

PHY AND PROTOCOL-AWARE TEST AND DEBUG

- Receiver margin testing requires calibrated insertion of various stresses for worst-case compliance testing:
  - Inter-Symbol Interference (ISI)
  - Random Jitter (RJ),
  - Common-Mode/Differential Mode Interference (CMI/DMI)

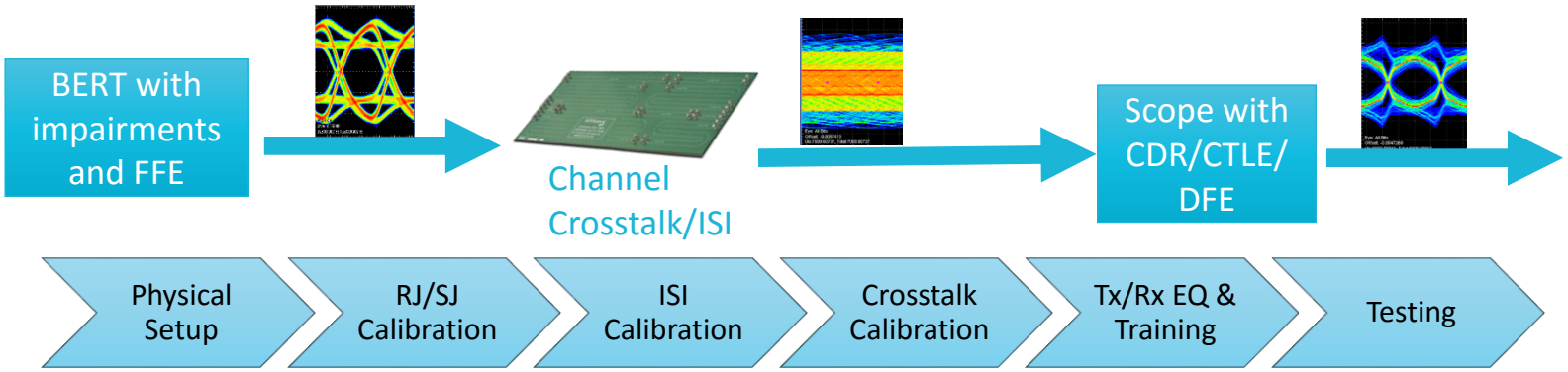
- Reference receiver models assist in calibrating compliance test conditions (eg Seasim/SigTest):
  - Models include the transmitted signal, applied stresses, and channel response to the receiver input pins



How to Address new Gen4 Challenges?

PHY AND PROTOCOL-AWARE TEST AND DEBUG

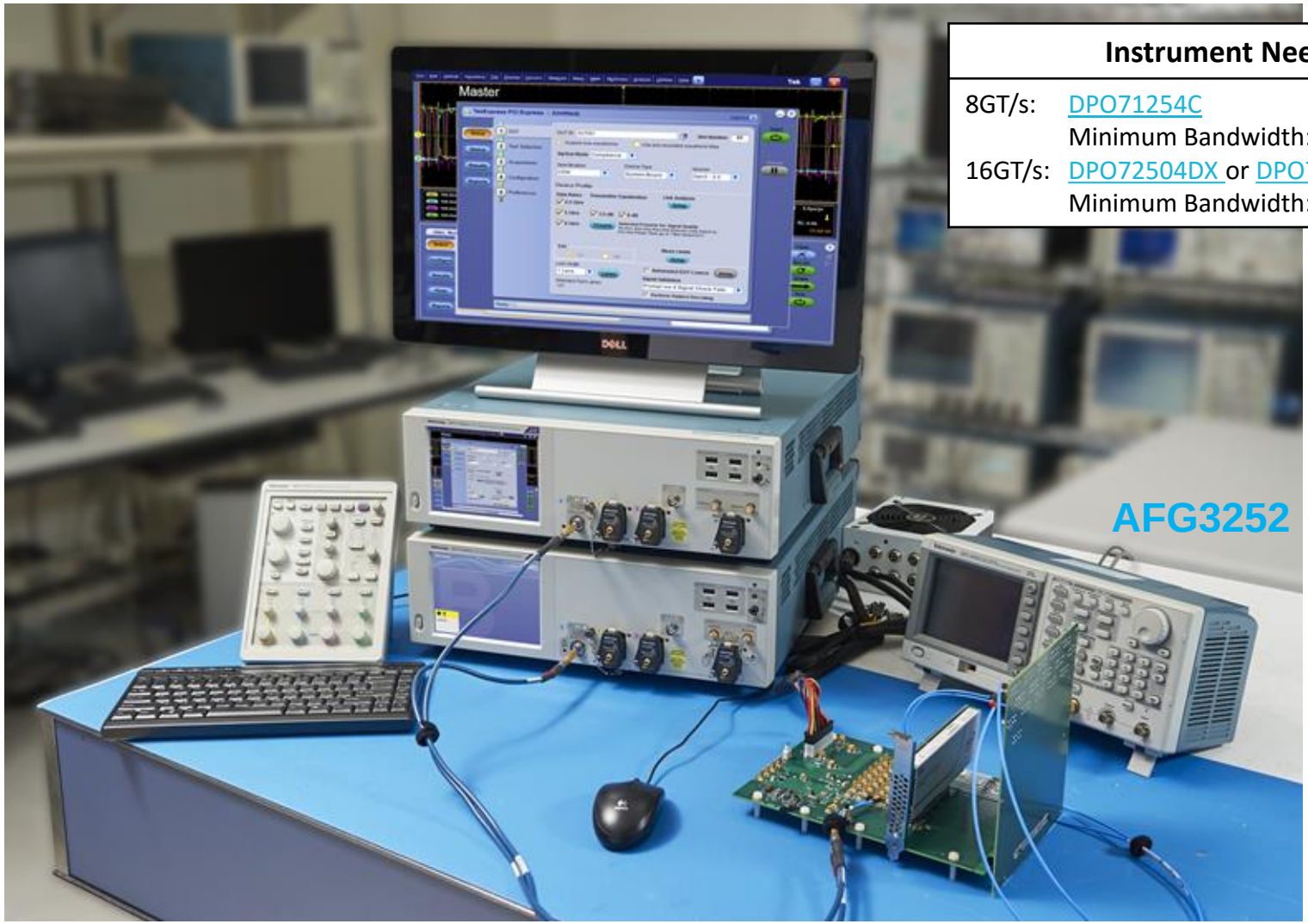
- Need fully integrated test system, including HW and SW solutions
  - Reliably put device under test into loopback mode
  - Facilitate link equalization training to optimize the channel, including built-in TXEQ and RXEQ optimization
  - Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
  - Debug DUT-specific problems with BER, FEC, and link training
- Solution must cover multiple standards (eg SATA, SAS, PCIe) and spec generations (eg Gen3, Gen4, etc)



Key Points in PCIe Test and Debug

- PCI Express (PCIe) will become the dominant storage interconnect in 2017.
  - New designs and players, broader customer implementation base, new specs to understand and apply, new compliance participation.
- A majority of PCIe Gen3 designs failed protocol compliance test at the first plugfest.
  - How will you verify protocol compliance on your device?
- Transmitter margin dependent on channel and optimized equalizer settings.
  - How will you verify actual transmitter margin meets design goals?
- Server environments will require repeaters or re-timers, essential for signal transmission over long lossy channels. These IC's double the number of equalization combinations possible.
  - How will you debug and perform interoperability test when repeaters/re-timers are present?
- Receiver lane margining tools will expose device performance and margin.
  - How will you verify actual receiver margin meets design goals?
- Custom high-speed serial interfaces will be used for application specific tasks.
  - How will you test your custom interface and verify operation to design goals?
- Receivers require unique external signal recipes to initiate test mode.
  - How will you establish loopback mode on your device to enable testing?

Tektronix PCIe Tx Solution

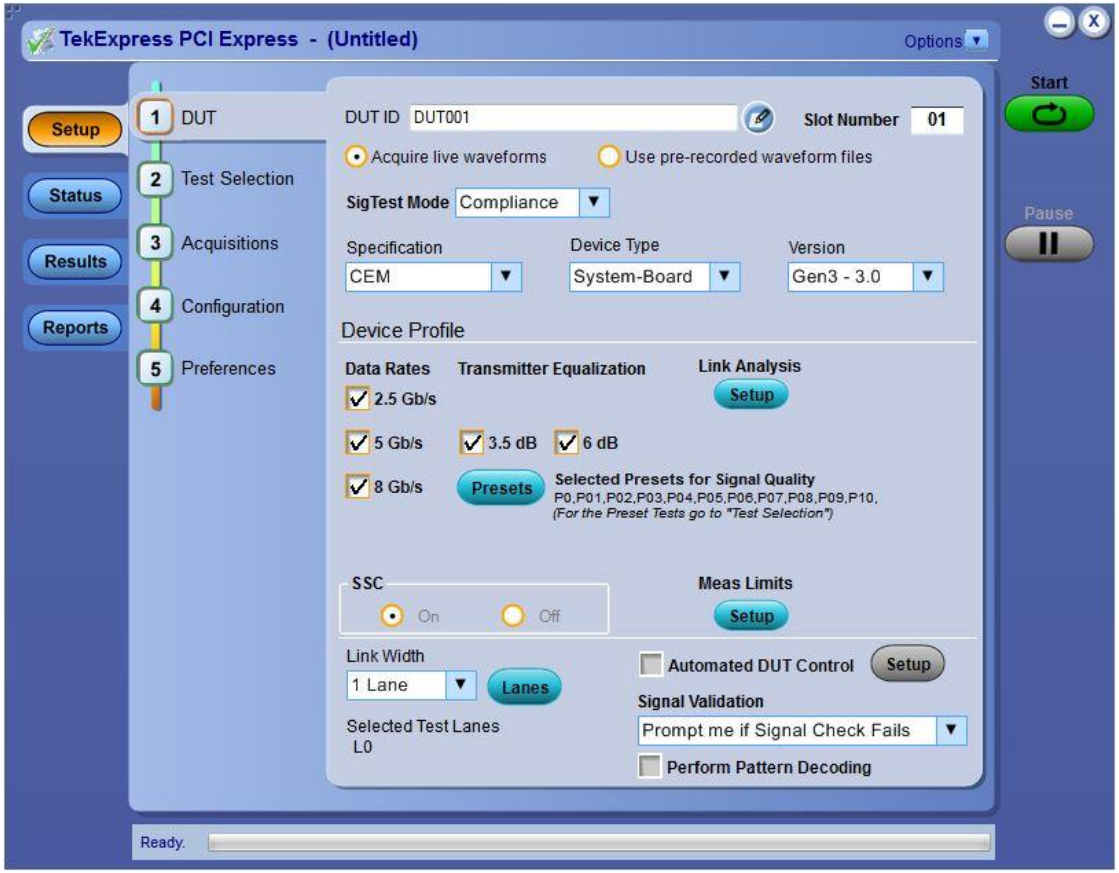


Instrument Needed	
8GT/s:	DPO71254C Minimum Bandwidth: 12.5GHz
16GT/s:	DPO72504DX or DPO73304SX Minimum Bandwidth: 25GHz

TekExpress for PCIe (Opt PCE4)

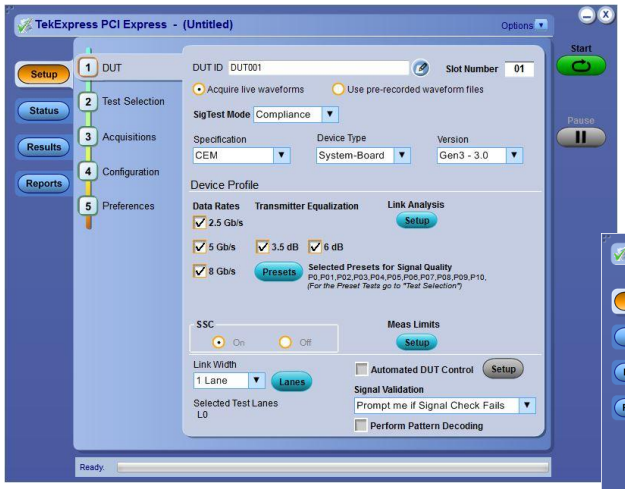
- TekExpress Automation for Tx Compliance with unique features including:

  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting

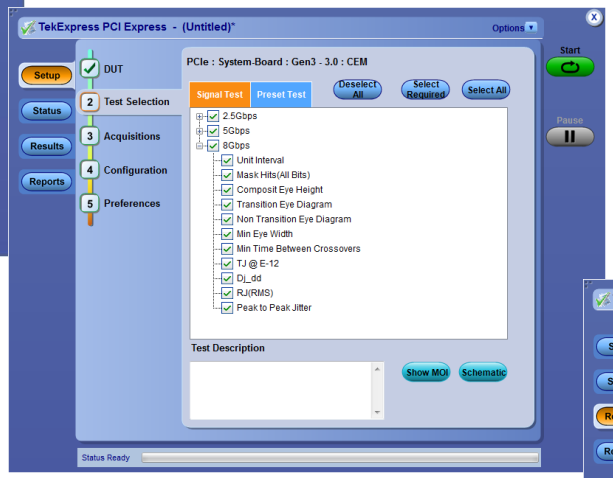


TekExpress PCIe Automated Test

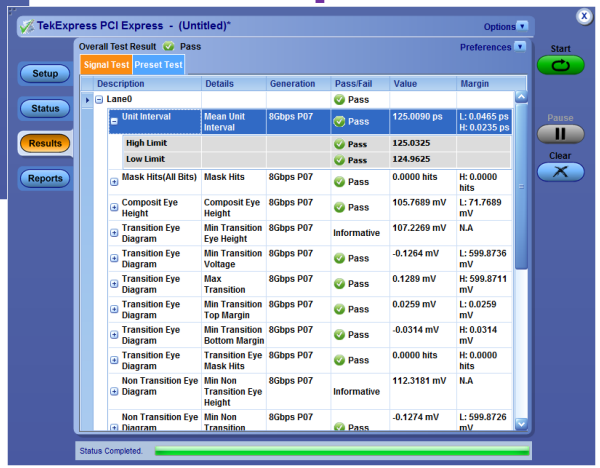
Setup



Test



Reports



Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

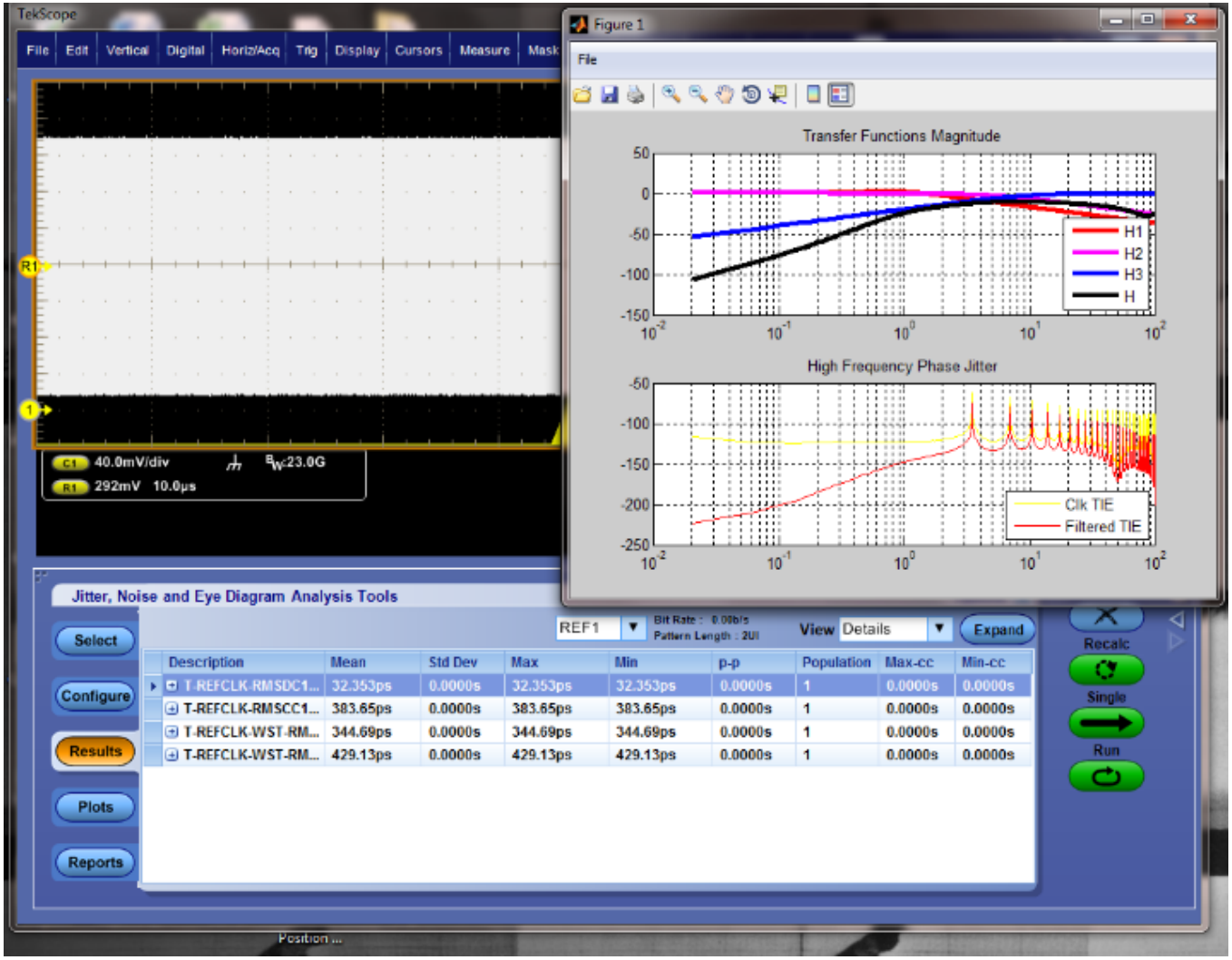
Automate DUT control

Test Selection

Standards-compliant pass/fail reports

DPOJet for PCIe Gen1-4 RefClk

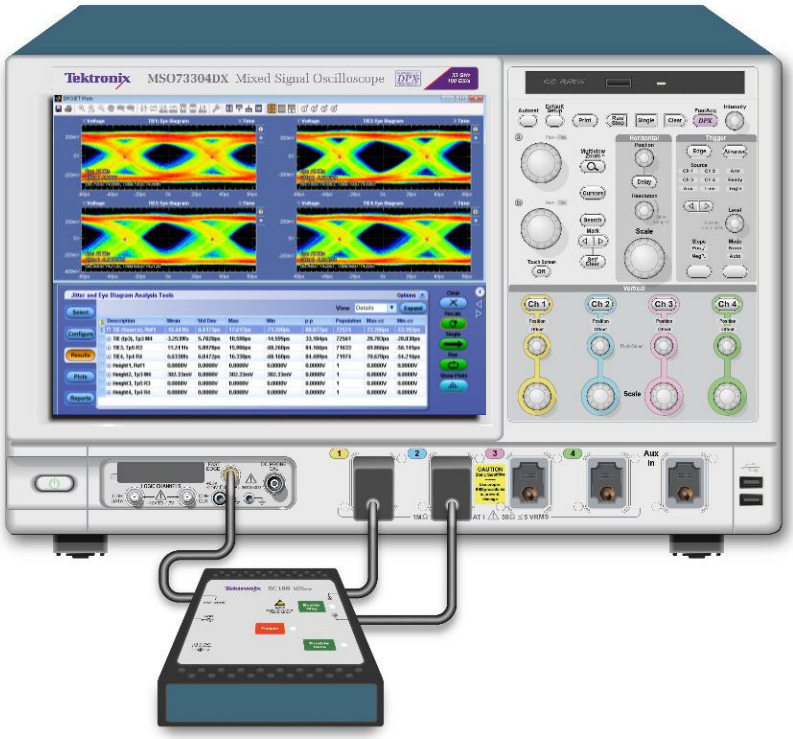
MEASUREMENTS

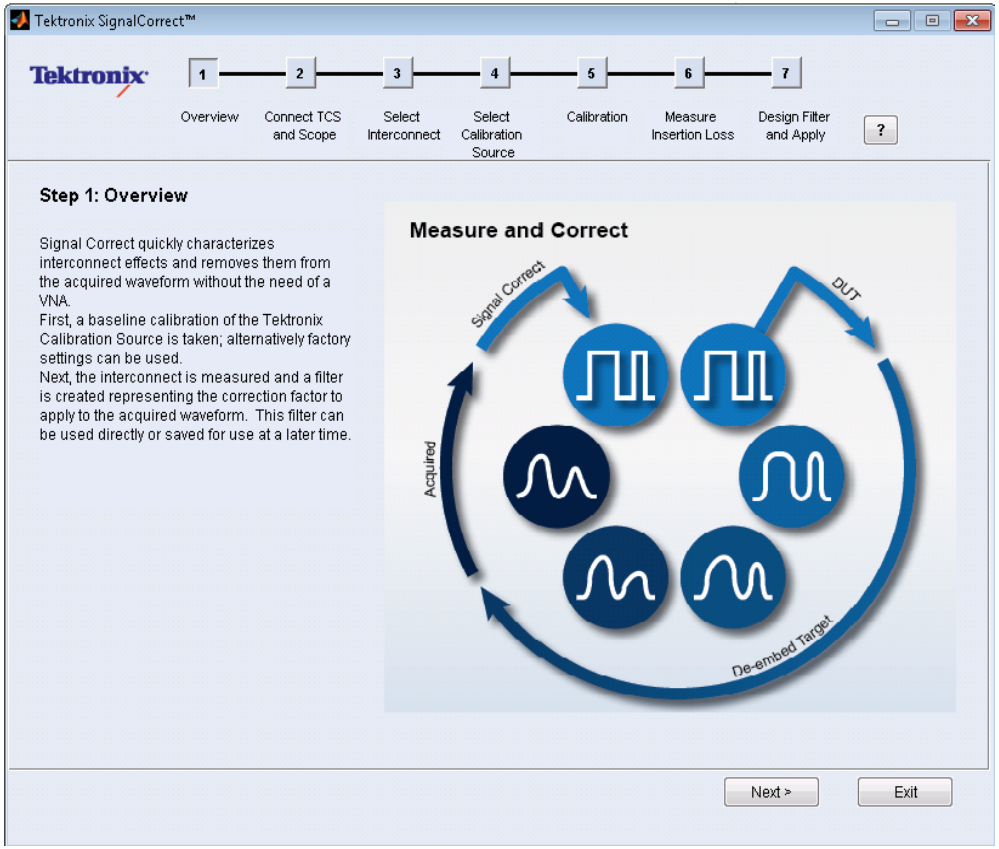


PCIe Decoder (Opt SR-PCIe)

- Provides link layer decoding
- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks

Channel Loss Characterization and De-embedding



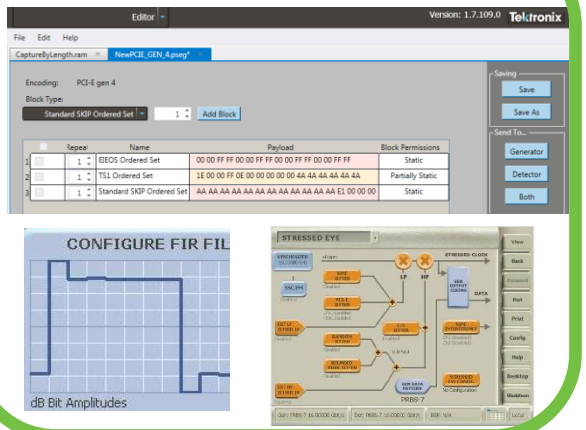


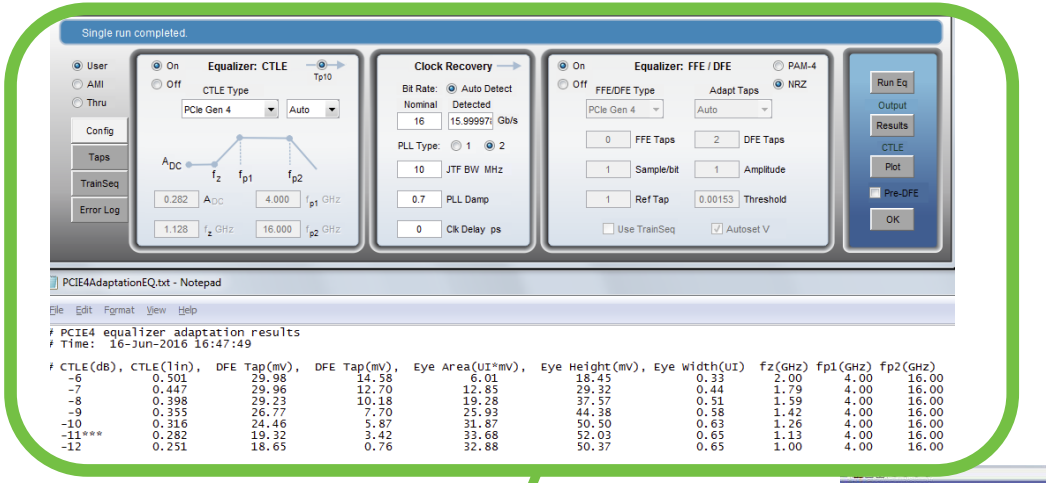
SignalCorrect: an easy to use solution that enables you to quickly characterize and de-embed the interconnect under test for more accurate measurement and analysis at much lower cost.

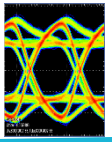
Tektronix Rx Test Solution

Introducing the BSX240 BERTScope

Key Elements in a PCIe Rx/Tx Link



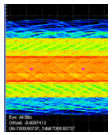




16GT/s

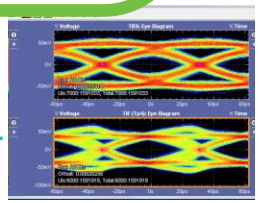
>20dB loss

Channel
Crosstalk/ISI



CTLE ONLY

CTLE + DFE



New BSX BERTScope with TXEQ, stress impairment, link training/handshaking

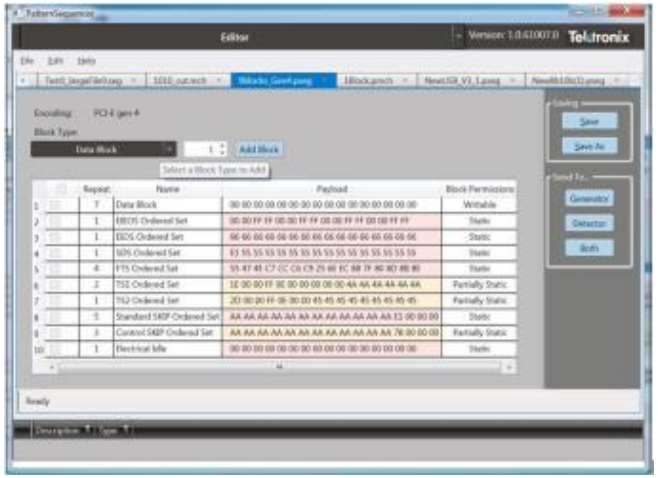
70K SX Scope with CDR + CTLE + DFE + Embed/De-Embed

Optimize
Calibrate
Automat

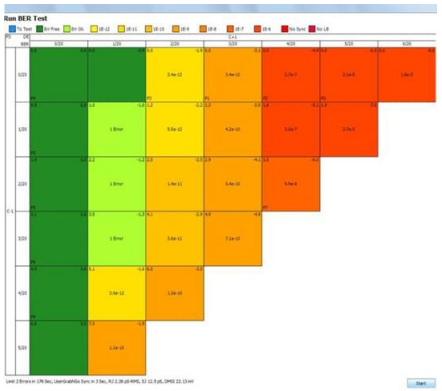
Debugging Loopback and Link Training

FROM COMPLEXITY TO CONFIDENCE

- **User Challenges:**
  - Preparing receiver for test**: reliably putting device under test into loopback mode and completing link equalization training to optimize the channel**
  - Debugging loopback and equalization failures



- **BSX Series BERTScope provides:**
  - Compliant link equalization training for PCIe Gen3 and Gen4
    - Fast internal control bus supports **500nS link training response time**
  - Handshaking support above 16Gb/s
  - Auto tuning and optimizing RxEQ settings via BER map

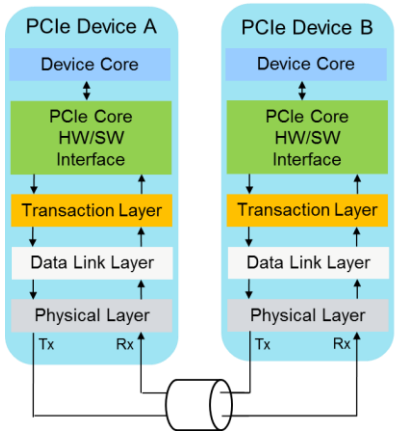


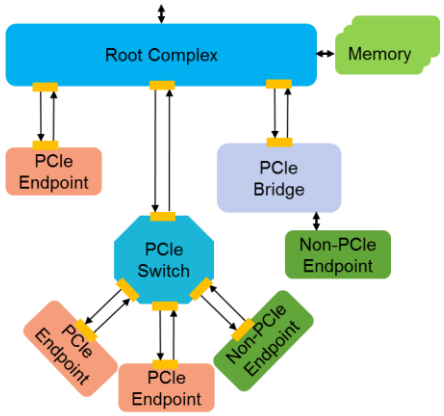
Debugging Loopback and Link Training

FROM COMPLEXITY TO CONFIDENCE

- Goal: Allow users to create their own **protocol-based patterns and link state traversals via stimulus-response feedback (protocol handshaking)**

- BSX Key Features:
  - Bit-oriented and protocol-oriented memory sequencer
    - Supports up to **128 states** and two levels of loop nesting
    - Sequence advancement by SW control, external signal, or Detector pattern match
  - Real-time data processing at **32 Gb/s**
  - Enhanced pattern/sequence editor
  - Stimulus-response feedback (handshaking)
    - Detector protocol pattern match -> Generator sequence advancement
    - Detector can match up to 16 user defined blocks
      - Up to 128 bits/block
    - Stimulus/response trigger output allows **cross-triggering of scope**

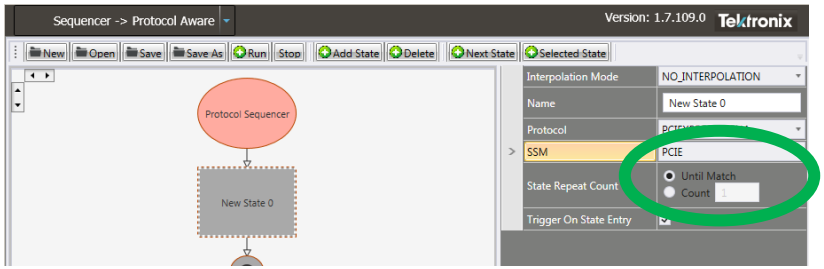


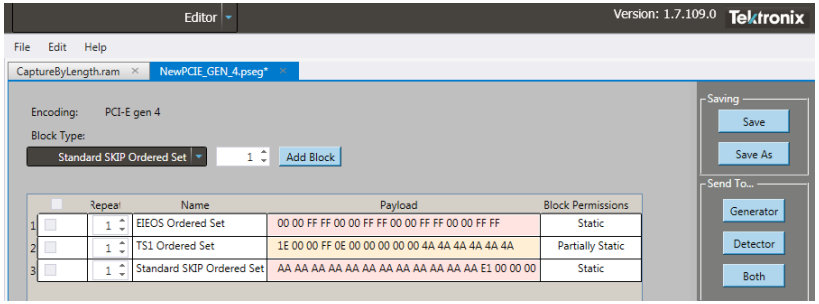


Debugging Loopback and Link Training

FROM COMPLEXITY TO CONFIDENCE

- In Protocol-Aware mode, pattern memory words are treated as protocol blocks or groups of symbols instead of bits
- Flexible partitioning of pattern memory
  - Supports multiple memory segments with looping capability
  - Memory size increased to 512 Mbits
- Includes bit-oriented and protocol-aware sequencing in generator
  - Protocol-aware detector pattern matching capability supports programmable protocol handshaking with the device under test.
- Memory contents may be transmitted by the generator with or without protocol processing (scrambling, encoding, etc)
- Words are fetched from memory and processed according to the selected protocol or encoding including:
  - Packaging of symbols into protocol blocks
  - Symbol encoding (ex: 8b/10b)
  - Data scrambling (all protocols)
  - DC balancing (PCIe Gen3/4, USB 3.1 SSP)

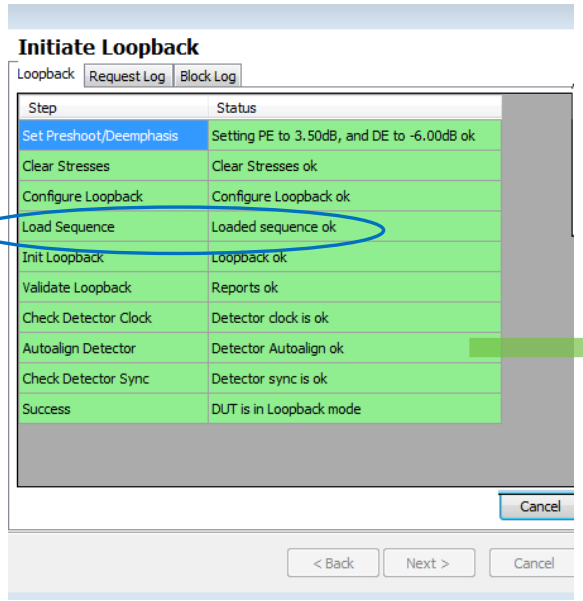


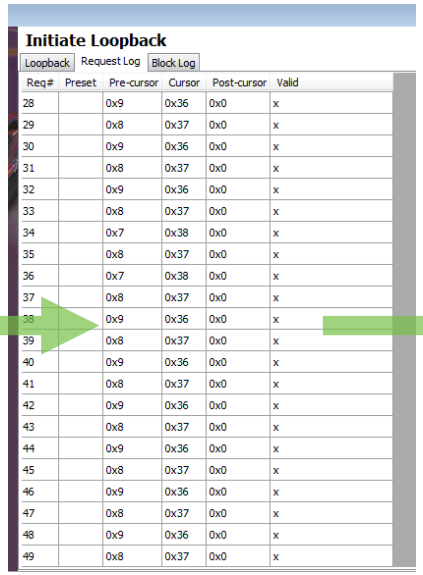


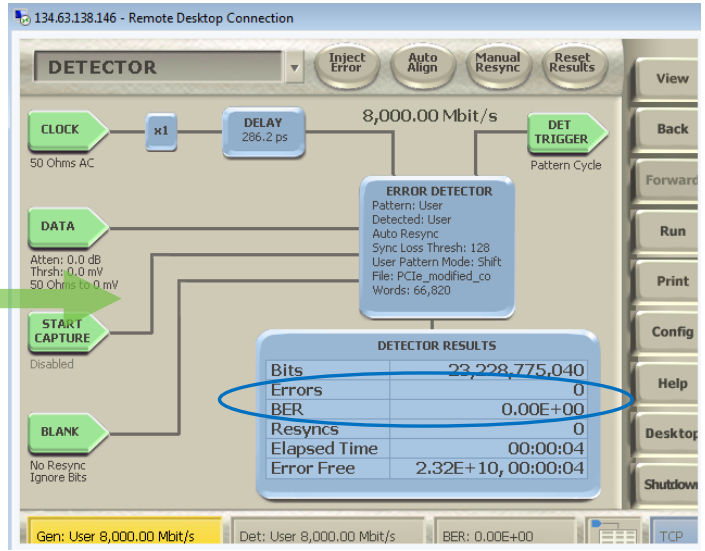
- Sixteen pattern match elements are available in Detector for protocol-based pattern matching
  - PCIe Gen3/4, USB 3.1 SSP
  - 8b/10b

Debugging Loopback and Link Training

FROM COMPLEXITY TO CONFIDENCE







Sequencer Loaded for PCIe Loopback Initiation and Debug

50 iterative requests from the DUT for TXEQ tuning

Error Free Operation Achieved!

Debugging Rx BER Failures

FROM COMPLEXITY TO CONFIDENCE

- **User Challenge:**
  - Need more than a bit-error rate (BER) number
  - Need to understand factors leading to bit error problems in order to debug issues

- **BSX Series BERTScope provides:**
  - “Scope” functionality that complement those of the Tektronix scopes
  - Full-featured and easy to use analysis tools
  - Eye diagram for quick diagnosis of synchronization and BER failure issues
  - Debug challenging signal integrity problems
    - Error Location Analysis
    - Pattern Capture
    - Jitter Map
    - BER Contour
    - FEC Emulation

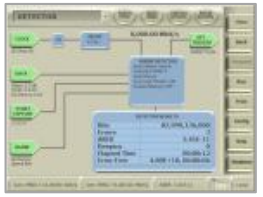

BER Contour

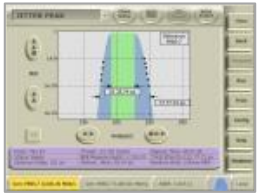

Eye Diagram


Error Location Correlation


FEC Emulation


Jitter Map


BER


Jitter


Jitter Tolerance

Tektronix Storage Test Solutions

FROM COMPLEXITY TO CONFIDENCE

Only with Tek…

Requires Protocol Awareness

…can you observe and debug protocol handshaking using a BERT at speeds up to 32Gb/s

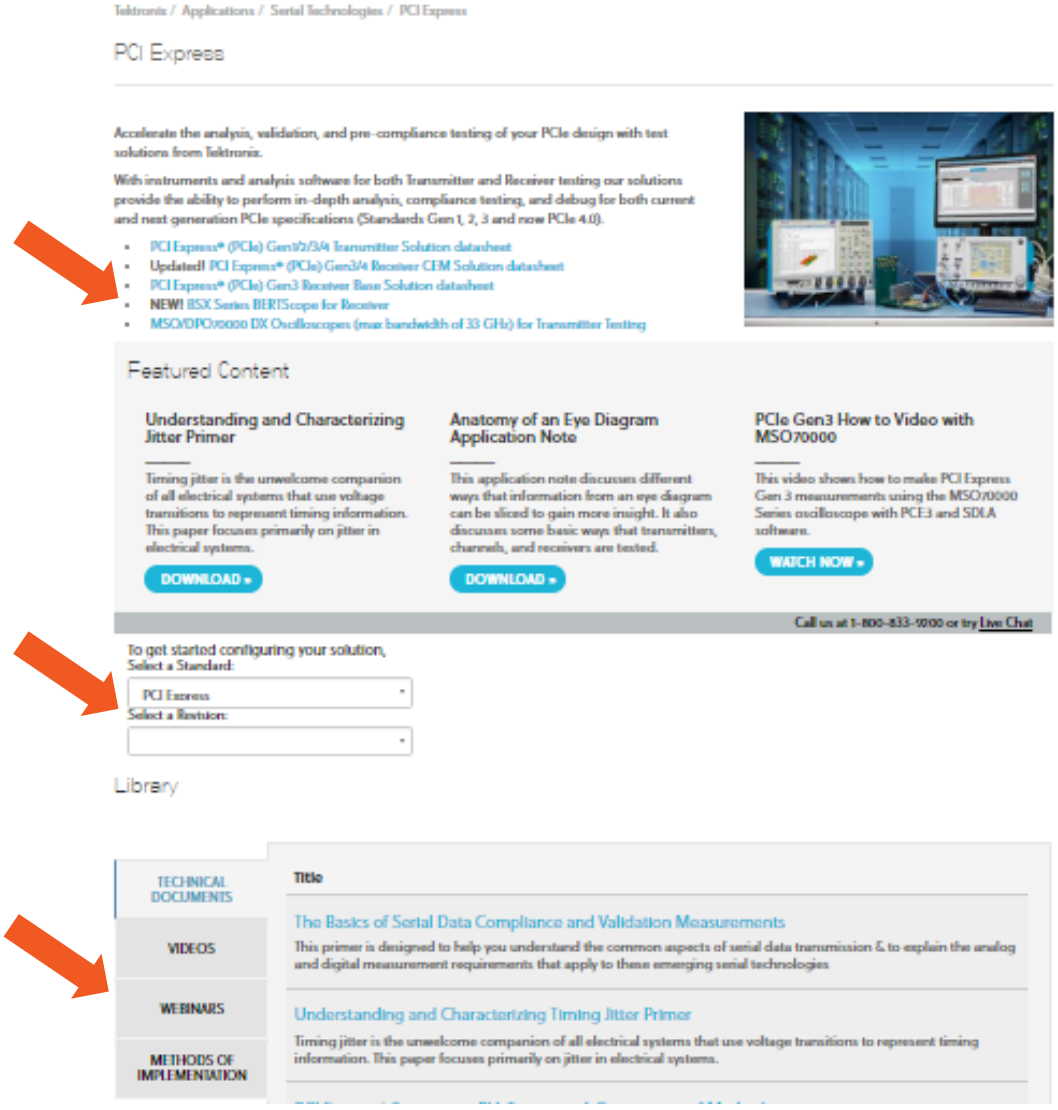
Need Automated Solutions for Gen3 and Gen4 Standards

…can you perform PCIe4 and SAS4 RX in-band testing using a single BERT
…can you automatically optimize CTLE/DFE settings
…can you fully automate PCIe compliance testing, reducing test time by over 2x

Go Beyond Compliance

…can you obtain Rx failure insight using BERT error location analysis
…can you use an Rx pattern sequencer to customize approaches for loopback initiation and link training
…can you quickly characterize channel insertion loss and de-embed its effects

www.tek.com/pci-express



Link to datasheets, MOI's, configurators

Tektronix PCIe solutions provide comprehensive Tx & Rx electrical PHY test coverage with integrated debug capabilities.